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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/824,344

04/15/2004

Hiroyuki Kanda

2004_0586A

6329

513 7590 10/10/2007
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EXAMINER

PATEL, TAYAN B

ART UNIT

PAPER NUMBER

1795

MAIL DATE

DELIVERY MODE

10/10/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/824,344

Applicant(s)

KANDA ET AL.

Examiner

Tayan Patel, Esq.

Art Unit

1795

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 4, 5, 6, 7, 8 of the present invention are rejected under 35 U.S.C. 102(b) as being anticipated by Basol et al. (US 6,943,112).

As to claim 1, Basol et al. discloses a plating method that prepares a substrate having relatively narrow recesses and a relatively broad recess defined in a surface (See Column 6, lines 24-30; See also Figure 2). Moreover, Basol et al. discloses a first plating under plating conditions for filling a metal in said narrow recess to form a plated film (See column 5, 35-56; See also Figure 2); electroetching or electropolishing by reversing the applied voltage (See column 9, lines 35-52). In addition, Basol et al. discloses a second plating under plating conditions for filling a metal in said broad recess (See columns 5-6, lines 57-67; See also Figure 2).

Art Unit: 1795

As to claim 2, Basol et al. discloses a method wherein the entire surface of said narrow recess and said broad recess are fully covered with a seed layer. See Column 1, lines 34-37.

As to claim 3, Basol et al. discloses a method wherein said first plating is performed under plating conditions for a relatively high bottom-up capability, and said second plating is performed under plating conditions for a relatively high leveling capability. See Column 9, lines 14-26.

As to claim 4, Basol et al. discloses a narrow recess with a width less than 0.2 micrometers and said broad recess has a width of 0.2 micrometers or greater. See Column 2, lines 31-37.

As to claim 5, Basol et al. discloses a substrate having a plurality of narrow recesses defined in the surface thereof. See Column 5, lines 35-37; See also Figure 1B.

As to claim 6, Basol et al. discloses a substrate having a plurality of broad recesses defined in the surface thereof. See Column 2, lines 31-37; See also Figure 2.

As to claim 7, Basol et al. discloses a first plating and second plating performed under plating conditions including different current densities upon plating. See Column 8 lines 54-65; See also Column 9, lines 20-22.

As to claim 8, Basol et al. discloses a second plating process performed under plating conditions including a current density higher than said first plating. See Column 8, lines 54-65; See also Column 9, lines 20-22.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 9 is rejected under 35 U.S.C 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Nagai et al. (US 2002/0027081).

With respect to claim 9, Basol et al. discloses all of the claimed limitations as discussed with respect to claim 8 above, yet fails to set the current density of first plating between 0.1 to 1.5 A/ dm², and a current density of second plating between 2 to 7 A/ dm².

Nagai et al. discloses an apparatus and method for plating a substrate with copper interconnects in order to fill recesses. In this reference, the first plating is performed at a current density between 0.1 to 1.5 A/dm² and the second plating is performed at a current density between 2 to 7 A/dm² in order to prevent the occurrence of burnt deposit and lower productivity. See Page 11, paragraph 0141; See also Page 9, paragraph 0124.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the current densities for the 2 plating steps in Nagai et al. in Basol et al. in order to prevent the occurrence of burnt deposit and lower productivity. See Page 9, paragraph 0124.

6. Claim 27 is rejected under 35 U.S.C 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Arya et al (US 4749454).

As to claim 27, Basol et al discloses all of the claimed limitations as discussed with respect to claim 1 above, further disclosing the processing of a semiconductor (See column 1, lines 10-13), yet fails to explicitly disclose the application of a reverse electric potential/bias for a period between 1 to 10 seconds.

Arya et al discloses the processing of a semiconductor (See column 1, lines 8-15) wherein a reverse-bias voltage is applied to 5-7 seconds (See column 5, lines 13-31) in order to improve the etching rate on the semiconductor device (See column 6, lines 15-67).

Art Unit: 1795

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the reverse-bias voltage of 5-7 seconds in Arya et al in the method of Basol et al in order to improve the etching rate on the semiconductor device.

Response to Arguments

102/103

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection necessitated by amendment.

Applicant argues that amended claim 1, now reciting the following limitations "applying a reverse electric field in a manner so as to etch the plated film in the narrow recess by said performing said first plating" is not obvious/anticipated over the prior art, namely, Basol et al in view of Taylor.

In light of applicant's amendment to claim 1, Examiner asserts that Basol et al discloses all of the claimed limitations as recited in amended claim 1. Applicant is referred paragraph 2 above, *supra*.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

Art Unit: 1795

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tayan B. Patel whose telephone number is (571) 272-9806. The examiner can normally be reached on Monday-Thursday, 7:30-5:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Neckel D. Alexa can be reached on (571) 272-9827. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TBP



ALEXA D. NECKEL
SUPERVISORY PATENT EXAMINER